DESIGN AND IMPLEMENTATION OF A TMS320C25-BASED HYBRID DIGITAL PHASE-LOCKED LOOP-AN APPLICATION TO TRANSPONDER RECEIVER BREADBOARD

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SUMMARY

The experimental study of a Phase-Locked Loop (PLL) with a digital loop filter is presented in this paper. Specifically, a TMS320C25 Digital Signal Processor (DSP) is used to implement this digital. loop filter. This PLL is designed and applied to the Deep Space Transponder (DST) receiver breadboard. In order to keep the compatibility, the main design goal was to replace the Analog PLL (APLL) filter within the DST receiver breadboard with a DSP--based digital loop filter without changing anything else. This replacement results in a Hybrid Digital PLL (HDPLL) . It is the first time that both DSP and HDPLL are employed in the DST receiver breadboard. Both the original APLL and DSP-based HDPLL are Type I, second order systems. The real-time performance of the DSP-based HDPLL and the receiver is provided and evaluated.

I. INTRODUCTION

Conventional. spacecraft transponders employ analog circuits from front end antenna to baseband carrier phase tracking loop. However, future NASA missions will require low cost, small sized, low power consumption spacecraft telecommunication equipment. To achieve the best design within mission resources, one must incorporate emerging technologies in the flight hardware. These requirements motivate a two-step approach. Firstly, before

buil ding a space-qualified all digital transponder, it is preferabl e to experiment on a simple and quick digital approach by using an existing X-band DST receiver breadboard in order to build confidence and obtain design experience. Consequently, a digital baseband sampling technique with a DSP-based HDPLL is proposed and applied directly to the existing DST receiver breadboard. Secondly, a bandpass sampling at Intermmediate Frequency (IF) technique with Application Specific Integrated Circuits (ASIC) is proposed as a full scale digital receiver with minimum power consumption.

The step one approach implies a quick experimental study of replacing a baseband analog loop filter by using a DSP-based digital filter in the PLL of the existing X-band DST receiver breadboard without changing anything else. It is the first time that both DSP and HDPLL are employed in the DST receiver breadboard . This paper presents both the implementation and experimental results of this DSP-based HDPLL and DST receiver breadboard.

The step two approach implies a higher sampling rate (i.e. digital IF) and advanced development. on digital receiver of DST. This will require to build a complete DST receiver which has less weight, small size, low-power consumption, and less cost. Consequently, the ASIC chip will be employed as digital hardware implementation rather than a DSP which may require higher power consumption in the spacecraft. An advanced DST receiver is currently under developing and results will be reported later on.

This paper describes the design, implementation, simulation, and real-time performance of a DSP-based HDPLL of the X-band DST receiver breadboard. The design specifications and functional. description of the carrier tracking loop are summarized in Section II. The conventional analog filter and APLL for various

input signal levels are given in Section III . Section IV describes digital filter design, the HDPLL, and analysis. Digital filter implementation and breadboard performance of the HDPLL are given in Section V. Finally, conclusions and recommendations are given in Section VI.

11. DESIGN REQUIREMENTS

The DST receiver specifications are listed as follows. The carrier signal tracking threshold is -157.3 dBm. The dynamic range is 88 dB (carrier threshold to -70 dBm) . The noise figure at DST receiver input is 1 .4 dB nominal. The tracking range is ±250 Khz minimum at the assigned channel frequency. The steady-state tracking error at a carrier signal level greater than -11.0 dBm shall be less than 1 degree per 40 Khz. The capture range is ±1.3 Khz at a carrier signal level greater than -120 dBm. The acquisition and tracking rate is at least 550 Hz/see at a carrier signal level greater than -110 dBm.

A DST receiver breadboard was built that met specifications using all. analog components in the APLL [1] . The carrier phase tracking APLL is a TypeI, second-order system with built-in characteristics, as follows:

1. The two-sided noise bandwidth ($2B_L$) of the carrier tracking loop at threshold is 18 Hz.
2. The Signal-to-Noise power Ratio (SNR) in the carrier tracking channel at the phase detector input is -25 dB.
3. The damping factor at threshold (-157.3 dBm) ranges from 0.4 to 0.6.
4. The loop predetection filter bandwidth is equal to 5000 HZ.

111. ANALOG PHASE LOCKED LOOP

The basic block diagram of the receiver breadboard of the DST is

given in Figure 1 (a) . The simplified APLL which tracks carrier phase is given in Figure 1 (b) . The equivalent HDPLL is obtained by replacing the analog loop filter with a digital filter, as shown in Figure 1 (b) and will be discussed in the next section. A bandpass limiter is used in the APLL and HDPLL receivers to maintain a constant total power at the input to the loop [2-3] . This minimizes the total mean square error of the loop over a wide range of input SNRS, It is also used to protect various loop components, the phase detector in particular, where signal and noise levels could otherwise vary over several orders of magnitude a:nd exceed the dynamic range of these components.

By measuring the analog loop filter of the DST receiver breadboard, the loop filter parameters τ_1 and τ_2 are obtained and its transfer function is given as follows:

$$F(s) = \frac{A_0(1+\tau_2 s)}{1+\tau_1 s} \tag{3.1}$$

where τ_2= 0.0464 see, τ_1=3655 see, A_0=43.4 dB.

Because the bandwidth of the loop predetection bandpass filter is 5 Khz, the threshold level at transponder input is -157.3 dBm. Consequently, the suppression factor α is 0.0531 at threshold and 1 at strong signal (50 dB above threshold) [2] . A detailed discussion on the suppression factor α is provided in Appendix I . The closed loop transfer function of the linearized APLL is given in [3] with open loop dc gain parameter k = $2.2*10^7$ [1] .

$$H(s) = \frac{1+\tau_2 s}{1+[\tau_2+\frac{1}{\alpha k}]s+\frac{\tau_1}{\alpha k}s^2} \tag{3.2}$$

For simulation purposes, the linearized APLL transfer function is computed for the input at threshold and strong signal . Computer

simulations are conducted for both cases. The magnitude and phase responses of the APLL are shown in Figures 2 (a) and 2 (b) at threshold and Figures 3(a) and 3(b) at strong signal , respectively . The damping factor is 0.5 for threshold and 2.18 :for strong signal from Figures 2 and 3, respectively. The two-sided equivalent loop noise bandwidth ($2B_L$) is 18 Hz at threshold and 160 Hz ($2B_L$) at strong input signal . Time domain responses of impulse, step, ramp error at both threshold and strong input signal. cases are shown in Figures 4(a)-(c) and 5(a)-(c), respectively.

The phase margins of the APLL are 44.5 degee and 85.6 degree at threshold and strong signal, respectively. Since phase is always greater than 180 degree, the gain margin is then not used. This APLL is a Type 1 system with $\tau_1 >> \tau_2$ and $\tau_1 >> 1$. Therefore, F(s) can be modelled as a perfect integrator as follows:

$$F(s) \approx \frac{A_0(1+\tau_2 s)}{\tau_1 s} \qquad (3.3)$$

This mathematical model of F(s) will be used to develop the equivalent digital filter in the next section for easy DSP implementation .

IV. DIGITAL FILTER DESIGN, THE HDPLL, AND ANALYSIS

The analog filter F(s) of the APLL is replaced by an equivalent digital filter and employed together with an Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) in the HDPLL as shown in Figure l(b) . A sampling rate must be selected first for the HDPLL. Since the 3-dB bandwidth of the bandpass limiter is 5 Khz and the DSP board employed provides the best Performance at a sampling rate of 50 Khz, the sampling rate is selected as *50* Khz. The higher the sampling rate *(50* Khz >> *5* Khz) , the more HDPLL performances like the analog loop.

IV.1. DIGITAL FILTER DESIGN

Two design steps are required to obtain digital filters. In step one, a digital filter algorithm must be developed. in step two, the digital filter coefficients must be quantized and scaled properly for fixed--point DSP implementation of the HDPLL.

IV.1.1. DIGITAL FILTER ALGORITHM

Based on the analog carrier loop filter transfer function, the bilinear transformation method is used to develop the digital filter [4,5]. Since the sampling frequency is much higher than the APLL noise equivalent bandwidth, the bilinear transformation method can be applied directly without prewarping the analog frequency. An alternative approach is to design digital filters by using s/z hybrid model for digital. PLLs as mentioned in [6] .

The Bilinear transformati.on is applied as

$$F_1(z) = F\ s)\ |_{s=\frac{2(z-1)}{T(z+1)}} = \frac{bz+c}{z-1} \qquad (4.1.1)$$

where $b = A_0(T+2\tau_2)/2\tau$ (4.1.2)

$c = A_0(T-2\tau_2)/2\tau_1$.

Parameters “b”, “c”, and associate zero of the digital filter are obtained and. given in Table 1.

Table 1. Parameters and zero of the digital filter

	parameter b	parameter c	zero
bilinear transformation	1.879256E-3	-1.878446E-3	.999569

Other transformation techniques such as impulse-invariant and hold equivalent (also known as step-invariant) are considered too. However, because the sampling frequency selected is much higher than the analog loop filter 3-dB bandwidth, results from these two techniques are almost the same as that of bilinear transformation. In general., the bilinear transformation is better than those two transformations in preserving the phase :response in the passband [11]. Hence $F_1(z)$ is chosen as the digital filter algorithm and will. be quantized for fixed-point DSP implementation.

IV.1.2. QUAIWIZATION AND SCALING [5]

Several simulations are conducted with fixed-point arithmetic in order to determine the number of bits of filter coefficients, digital gain, and scaling factor for implementation, Because the analog loop filter has an extremely narrow bandwidth in comparison to the sampling frequency, the pole and zero of the corresponding digital filter may be cancelled out each other if improper scaling and quantization applied. Finally, 16-bit coefficients and a digital gain (g_d , 148) are selected for the following reasons:

1. For easy and fast acquisition,
2. Accurate digital representation for parameters “b’ and "c" and to avoid pole-zero cancellation due to quantization,
3. Easy implementation by a TMS320C25,
4. To preserve the noise equivalent bandwidth by choosing g_d = 148 for both strong signal and threshold. More discussion on the g_d is provided in the analysis section.

The 16-bit digital filter is obtained as

$$F_q(z) = \frac{[b_q z + c_q] 2^{-8}}{z - 1}. \qquad (4.1.3)$$

where

b_q = {Int [$(g_d b/A_0)\ 2^{8}*2^{15}$ - 1)+.5]}/$(2^{15}-1)$ = *15764/32767*

c_q = {Int[$(g_d c/A_0)2^{8}*2^{15}$ - 1)+.5]}/$(2^{15}-1)$ = *-15758/32767*

g_d = digital gain = *148*

Int [.] represents the integer portion of [.] .

This digital filter exhibits similar performance to the analog carrier loop filter. However, an extra 8-bit gain (2^8) is applied to form b_q and c_q in equation (4.1 .3) for maximizing numerical accuracy and results in 16-bit fixed-point coefficients for DSP implementation. This 8-bit gain is then compensated by 2^{-8} at the output of the digital filter. Hence the total filter gain remains the same as that of the analog filter. Notice that distortion due to quantization is very small and can be ignored.

IV.2. THE DSP-BASED HYBRID DIGITAL PHASE LOCKED LOOP

The simplified block diagram of a DSP-based HDPLL is shown in Figure 1 (b) . Equation (4.1.3) will be implemented as the fixed-point digital filter F(z) . By comparing Figures 1 (a) and 1 (b), one notes that the analog filter of Figure l(a) is replaced by an equivalent digital filter with the 16-bit ADC and DAC in Figure 1(b). We model the ADC plus digital filter plus DAC as an impulse modulator, a fixed-point digital filter algorithm, and a zero-order hold. By using the block diagram analysis of sampled data systems [4], the sampled (discrete-equivalent) transfer function, H(z), of the linearized HDPLL is obtained. A detailed derivation is given in Appendix II. Again, computer simulations are conducted at both threshold and strong signal cases . The magnitude and phase responses of the DSP-based HDPLL are shown in Figures 2(a) and 2(b) at threshold, and Figures 3(a) and 3(b) at strong signal, respectively. Frequency responses of the APLL and HDPLL are approximately the same except, the phase response at frequencies above 1 Khz. This shows that the designed HDPLL preserves both magnitude and phase characteristics very well at frequencies less than 1. Khz. Consequently, the noise equivalent

.1 oo-p bandwidth of the HDPLL is the same as that of the APLL at both strong signal and threshold cases, Therefore, the phase jitter of the HDPLL is the same as that of the APLL.

The impulse, step responses, and ramp error response of the DSP-based HDPLL at both threshold and strong signal cases are shown in Figures 6(a)-(c) and 7(a)-(c) , respectively. The ramp error response shows the Dynamic Phase Error (DPE) in the acquisition. The digital gain is 148 at threshold in Figures 6(a)-(c). Two different digital gains are used in Figures 7(a)-(c) . Notice that time domain responses of the HDPLL are significantly different from counterparts of the APLL. Specifically, the impulse response of the HDPLL has a much smaller dynamic range than that. of the APLL. On the other hand, the DPE of the HDPLL has a much larger dynamic range than that of the APLL. However, the impulse response of the HDPLL becomes larger with a larger digital gain as shown in Figure 7(a) . The DPE becomes smaller with a larger digital gain as shown in Figure 7 (c) . This means that digital gain significantly controls the dynamic range of the time domain response. These features indicate that the dynamic range of the accumulator of the processor must be large enough to accommodate the DPE during the acquisition process. We select g_d = 148 for having a B_L which meets the specification. Step responses of the HDPLL, Figures 6(b) and 7(b), show that. the damping factor is about . 5 at threshold and larger than 1 at strong signal. Notice that there is a smoothing analog filter used after D/A in the HDPLL. Consequently, this HDPLL is a Type 1", 2nd order closed loop system.

IV.3. ANALYSIS

In general, it doesn't matter whether the gain is in the digital or analog portion of the HDPLL. However, since all analog parts of the HDPLL are fixed components in the receiver breadboard, only the digital filter gain can be easily adjusted as a flexible parameter in the DSP. Consequently, the digital. gain becomes an

important parameter which controls the stability, phase and gain margins, and the noise equivalent bandwidth.

IV.3.1. DIGITAL GAIN VS. STABILITY

It is well known that second order, Type I APLLs are unconditionally stable. However, Type I HDPLLs are only conditionally stable and Type I second order HDPLLs are unstable at high loop gains. The root locus plot of the HDPLL is shown in Figure 8. Both poles are forced to remain on or near the real axis for the maximum possible range of loop gain as shown in Figure 8. The pole of the HDPLL moves outside unit circle and becomes unstable when digital gain is larger than 50465. By using g_d = 148, the phase margin and gain margin of the HDPLL is computed at both threshold and strong signal cases. Table 2 compares the phase margin between the APLL and the HDPLL.

Table 2. A comparison of phase margin and gain margin between the APLL and HDPLL.

	Phase Margin		Gain Margin	
	APLL	HDPLL	APLL	HDPLL
Threshold	44.5°	47°	N/A′	-77dB
Strong Signal	85.6°	86°	N/A″	-51dB

′ Gain margin is not used because the phase of APLL is always greater than 180 degree.

The phase margin of the HDPLL is about. the same as that of the APLL . Consequently, the HDPLL is very stable at both threshold and strong signal cases.

IV.3.2. DIGITAL GAIN VS. NOISE EQUIVALENT BANDWIDTH

The one-sided noise equivalent digital bandwidth B_{Ld} (Hz) of the HDPLL is given by

$$B_{Ld} = \frac{1}{2T * H^2(1) * 2\pi j} \oint_{|z|=1} H(z) H(z^{-1}) \frac{dz}{z} \qquad (4.3.1)$$

where T is the update time in seconds, and H(z) is the transfer function of the HDPLL with H(1)=1. The B_{Ld} can be calculated by using either numerical integration or Table III in [7] . At g_d = 148, the $2B_{Ld}$ is obtained as 156 Hz and 17 Hz at both strong signal and threshold, respectively. The noise equivalent. bandwidth of the HDPLL is nearly the same as that of the APLL. Furthermore, the relationship between the g_d and the B_{Ld} is depicted in Figure 9 at strong signal case. Figure 9 shows the noise equivalent loop bandwidth increases when digital gain increases . However, the B_{Ld} will be greater than 25 Khz if the digital. gain is greater than 26400. Consequently, the g_d should be less than 26400 to avoid aliasing errors.

IV.3.3. STEADY STATE PHASE ERROR [8]

Under the assumption of linearity, the phase error (no noise) in the z-domain is given by the following expression:

$$\Phi(z) = \{1 - H(z)\}\theta_i(z) \qquad (4.3.2)$$

where H(z) is the closed loop transfer function of the HDPLL and $\theta_i(z)$ is the z-transform of the phase input. Furthermore, an instantaneous doppler denoted as d(t) is assumed as

$$d(t) = \omega_i(\Omega_0 + \Lambda_0 t)/c \qquad (4.3.3)$$

where ω_i . carrier frequency (rad/see)
Ω_0 = spacecraft speed (m/see)
Λ_0 = spacecraft acceleration (m/sec^2)
c = speed of light (m/see) .

The input phase $\theta_i(t)$ of the HDPLL is the integration of the d(t) with respect to time and is obtained by

$$\theta_i(t) = \omega_i(\Omega_o t + 0.5\Lambda_o t^2)/c. \qquad (4.3.4)$$

By applying the final value theorem to the phase error equation, we get

$$\begin{aligned}\phi_{ss} &= \lim_{z\to 1}(z-1)(1 - H(z))\theta_i(z) \\ &= \lim_{Z\to 1}(z-1)(1-H(z))(\omega_i/c)[\Omega_o Tz/(z-1)^2 + 0.5\Lambda_o T^2 z(z+1)/(z-1)^3]. \\ &= (\omega_i/c)\Lambda_o T/[(k/A_0)(b_q+c_q)2^{-8}] \qquad (4.3.5)\end{aligned}$$

For the Cassini mission at an 8.4 Ghz carrier frequency, we assume accelaration values of $\Lambda_o = 2$ m/sec^2 for Saturn. The steady state phase error at. strong signal case is obtained as .607 degree at encounter. Clearly, this HDPLL meets the specification which requires a steady state phase error of 1 degree, as mentioned in Section II .

IV.3.4. THE PHASE ERROR VARIANCE OF THE PLL

The phase error variance of the linearized APLL after the bandpass limiter is calculated as

$$\sigma_e^2 = (N_0 B_L/P_c)\Gamma$$

where NO = the one-sided noise power spectral density,
P_c = the carrier power,
Γ = limiter performance factor = $(1+\rho_i)/(0.862+\rho_i)$,
$\rho_i = P_c/N_0 W_i$ = the SNR input to the limiter.
W_i = the bandwidth of the bandpass filter = 5 Khz.

The limiter performance factor equation is obtained experimentally [9] . From the breadboard DST second IF gain

distribute. on measurements, parameters of Table 3 are obtained with the Automatic Gain Control (AGC) on (threshold) and off (strong signal), respectively.

Table 3. Measured signal and noise power input to the limiter, and associated parameters ρ_i and Γ at threshold and strong signal.

	P_c	N_0W_i	ρ_i	Γ
Threshold	-26.5 dBm	-1.5 dhm	0.003	1.16
Strong Signal	-26.5 dBm	-87.5 dBm	$1.2*10^6$	1

Based on the parameter provided in Table 3, the SNR of both the APLL and HDPLL can be computed as follows.

SNR of the APLL = $10\log(1/\sigma_e^2)$ dB

$= 10[\log(P_c/N_0W_i) - \log(\Gamma) + \log(5000/B_L)]$ dB

SNR of the HDPLL = $10\log[1/((N_0B_{Ld}/P_c)\Gamma)]$ dB

The measured SNR of both APLL and HDPLL at both threshold and strong signal is provided in Table 4.

Table 4. The measured SNR of both AI'LL and HDPLL at both threshold" and strong signal.

	SNR-APLL (dB)	SNR-HDPLL (dB)
Threshold	1..80	2.05
Strong Signal	78.96	79.07

*Measured threshold is defined as the point where probability is 50% lock and 50% unlock.

"V. DIGITAL FILTER IMPLEMENTATION AND BREADBOARD PERFORMANCE

A PC board of the Ariel DSP-16 Plus is employed together with an X-band DST breadboard for real-time digital loop filter implementation. Bandwidth of both antialiasing (input) and smoothing (output) filters is 20 Khz. Both ADC and DAC are 16-bit with a selected sampling rate of 50 Khz for best board performance. A TMS320C25 digital signal processor is employed to implement this 16-bit digital loop filter. This DSP has a 32-bit wide accumulator. However, a 40-bit equivalent. accumulator is employed to accommodate the large dynamic range required during the acquisition process.

Transponder receiver experiment results are obtained in real-time operation. Evaluation experiments include receiver tracking threshold sensitivity and static phase errors for X-band uplink frequency offset. All measurements were made at room temperature (25°C). The theoretical equation used for the calculation of carrier tracking threshold is given in Appendix I. The measured tracking threshold sensitivity at the receiver best lock frequency (71.62.3125 Mhz) is -155.3 dBm which is higher than the design threshold value of -15"7.3 dBm. This is due to the DC bias at the A/D of the DSP board. However, the measured hybrid digital receiver threshold characteristics show good correlation with the actual analog receiver performance and agree to theoretical. performance over the tracking range, as shown in Figure 10. Figure 11 shows a linear relationship for the measured Static Phase Error (SPE) voltage versus uplink frequency offset over the receiver tracking range. The measured SPE shows a good correlation with expected performance (Appendix III). The measured tracking ranges of the APLL and HDPLL are ±270 and ±280 Khz, respectively, which is greater than the requ: red tracking range value of ±250 Khz.

V. CONCLUSION

This artical presents the design, implementation, analysis, and performance testing of a DSP-based HDPLL of the DST receiver breadboard. The baseband carrier loop filter has been successfully replaced by a 16-bit digital filter (digital integrator) . A TMS320C25 DSP is employed to implement this filter in real-time. All simulations show that the designed fixed-point digital filter works very well in the HDPLL. The simulated performance in the frequency domain of the HDPLL is nearly the same as the original APLL at both threshold and strong signal cases. However, time-domain responses of the HDPLL are controlled by the digital gain. To meet the B_L requirement, the g_d is chosen as 148. Hence, the HDPLL's dynamic range of time domain responses is different than that of APLL.

Testing results are in good agreement with predicted characteristics, with the exception of tracking threshold (about. 2 dB loss due to the DC bias of the baseband A/D) . This loss can be reduced if the digitization occurs at the IF signal, instead of the digitizing baseband signal . In conclusion, it has been demonstrated that the baseband carrier loop filter of the DST receiver can be replaced by a digital filter. By using this DSP-based HDPLL as a basic model, an advanced digital receiver which employs digital IF and ASIC is currently under developing [10-11] . An adaptive scheme is also recommended to solve the high transient DPE problem as follows. First, to reduce the transient DPE in the acquisition mode, the digital gain of the digital filter should be increased. Consequently, the loop bandwidth is opened up. This operation will ensure a larger acquisition sweep rate. Secondly, after the phase is locked, the digital gain should be reduced. Hence, the loop bandwidth is reduced in the tracking mode. This operation will reduce phase noise.

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APPENDIX I. A Mathematical Model of the Suppression Factor and Tracking Threshold Calculation

The carrier tracking threshold [2,3], [12,13] of a PLL receiver is defined as the minimum uplink signal. required to maintain a 50% probability of lock and 50% probability of unlock at any given offset from best. lock frequency (BLF) . The worst case carrier tracking threshold signal level SO at the transponder input port and at the BLF is determined from the following equations (AI.1 - AI.5) .

$$SO = kT_oF(2B_L)L \qquad \text{(AI.1)}$$

where SO = the received input signal level for tracking threshold at receiver BLT,

k = Boltzmann's constant,

T_o = the reference system temperature,

F = receiver noise figure at the transponder input,

L = the receiver carrier channel loss.

The SO is calculated and equal to -157.5 dBm (the receiver carrier tracking threshold) for a $2B_L$ of 18 Hz, channel loss of 1 dB, and noise figure of 2.9 dB at, 290 K.

The PLL receiver limiter suppression factor α [2,3], [1.2], is given by

$$\alpha = 1/\sqrt{1+[2B_{LI}S_o/\pi B_L S]} \qquad \text{(AI.2)}$$

where S = the receiver input signal power level,

B_{LI} = the noise equivalent. predetection bandwidth.

In the region near tracking threshold, the phase offset, θ_e, at the PLL phase detector can be estimated **from an empirical equation:**

$$\theta_e = 1 - \alpha_0/\alpha \qquad \text{(AI.3)}$$

$$\alpha_0 = (\pi B_L/2B_{LI})^{0.5}$$

Notice that α_0 is the limiter suppression factor at carrier threshold.

The phase detector output voltage is given by an empirical equation

$$V_c = \alpha \sin(\theta_e)\cos(\theta_e) . \qquad \text{(AI.4)}$$

The frequency offset at X-band is then obtained as follows.

$$\Delta f = V_c k \qquad \text{(AI.5)}$$

where k = o:pen loop DC gain of the PLL.

APPENDIX II . Derivation of the HDPLL Closed-Loop Transfer Function

From Figure 1(b), the DAC is modeled as $(1-e^{-sT})/s$, and the Voltage-Control led Oscillator (VCO) is modeled as k/s. Then the output of the sampled-data system is obtained as

$$\theta_o^* = \frac{G''}{1 - t\, G^*}\, \theta_i^* \qquad \text{(AII .1)}$$

where

θ_o^* = the sampled output. of the HDPLL

θ_i^* = the sampled input of the HDPLL

$G' = \alpha(1-e^{-sT})F_q^*((k/g)/s^2)^*$

$= \alpha(1-e^{-sT})F_q[T(k/g)e^{sT}/(e^{sT}-1)^2]$

$$\frac{AF_q(z)}{z-1}$$

$$= \frac{A(b_q z + c_q)}{(z-1)^2} \qquad \text{(All .2)}$$

and $A = \alpha k T 2^{-8}/g$

$z = e^{sT}$

b_q and c_q are 16-bit digital filter coefficients.

The closed loop transfer function is then

$$H(z) = \theta_o^*/\theta_i^* = A(b_q z + c_q)/[z^2 + (Ab_q - 2)z + Ac_q + 1]\,. \qquad \text{(AII.3)}$$

APPENDIX III. Relationship Between SPE and Uplink Frequency Offset

The relationship between the static phase error (SPE) and the uplink frequency offset over the receiver tracking range is found as follows.

The VCO receives SPE as input and provides output frequency at $12F_1$ with a gain of 628 Hz/volt (measured) . The frequency of the received uplink signal is $749F_1$ as shown in Figure 1 (a) . Consequently, the uplink frequency offset from the best lock frequency is obtained as

$$\Delta f = - SPE*628*749/12.$$

The "-" sign is used for the negative feedback PLL.

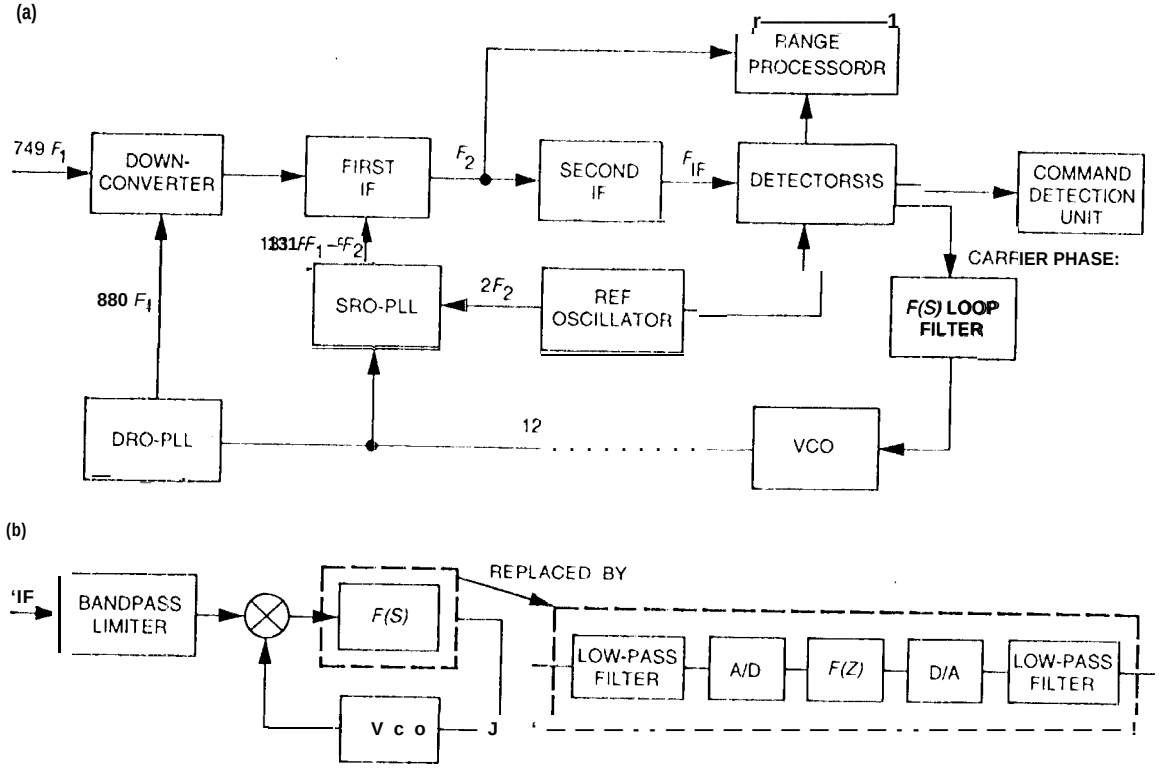


Fig. 1. Functional block diagrams of (a) the receiver of the DST breadboard and (b) the simplified carrier phase tracking loop with the analog loop filter replaced by a digital filter.

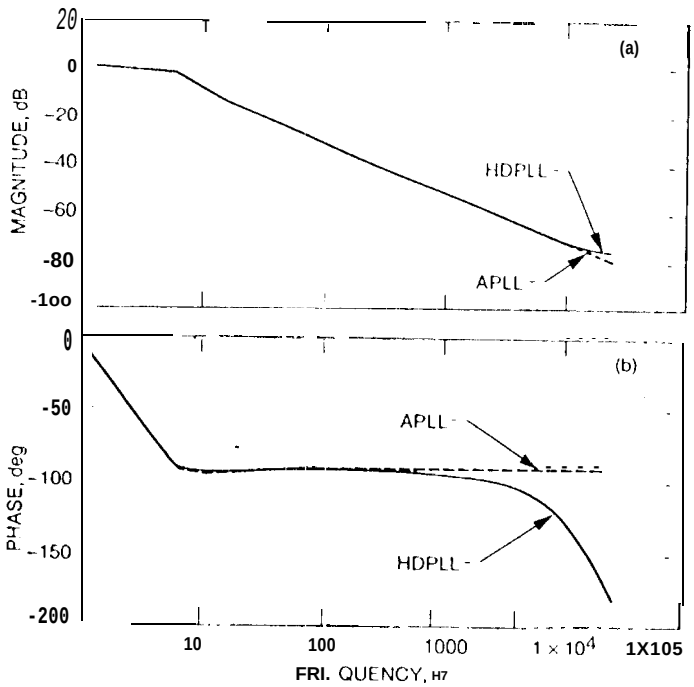


Fig. 2. Simulated responses of the APLL and HDPLL at the threshold: (a) magnitude and (b) phase.

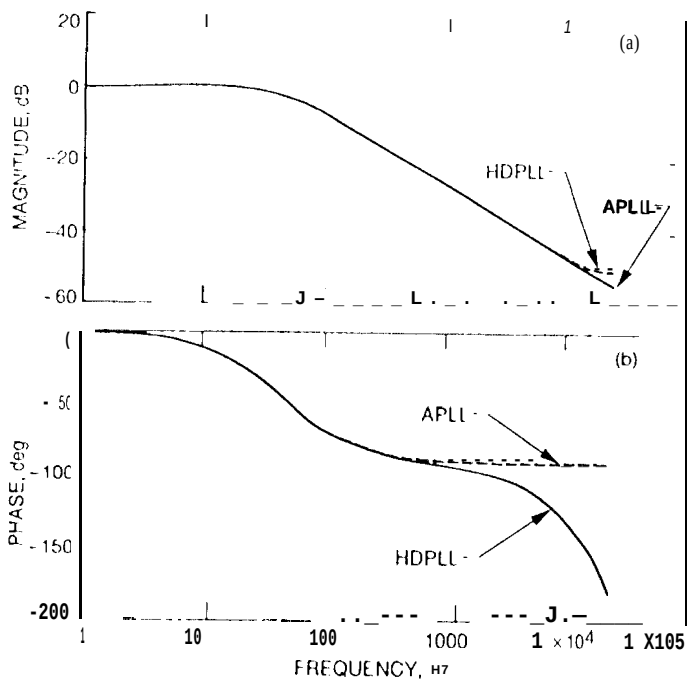


Fig. 3. Simulated responses of the APLL and HDPLL at the strong signal input: (a) magnitude and (b) phase.

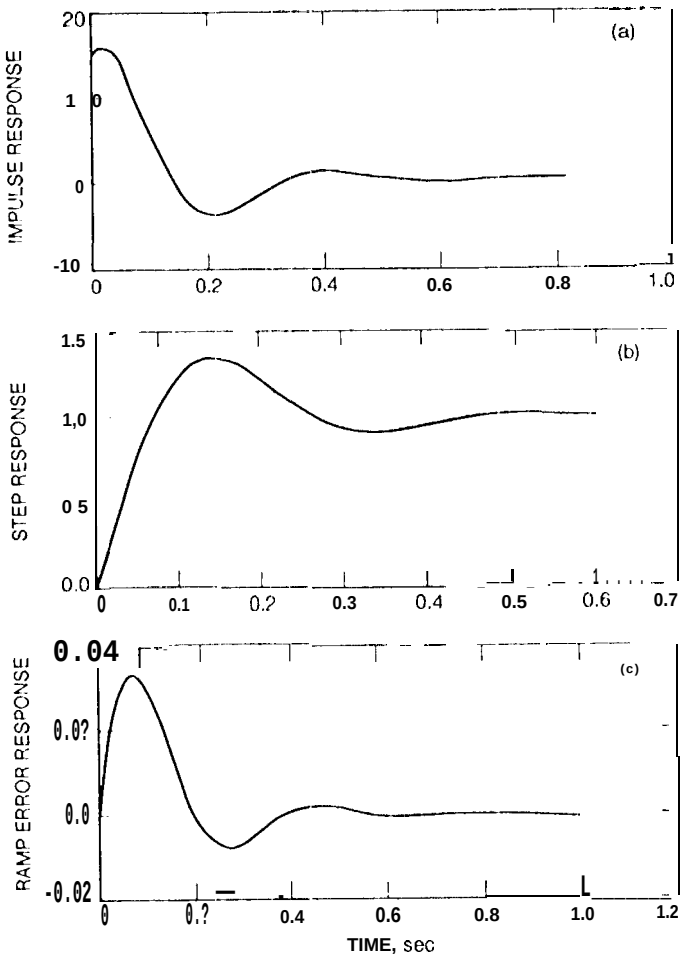


Fig. 4. Time-domain reaponaea of the APLL at threshold: (a) impulse, (b) step, and (c) ramp error.

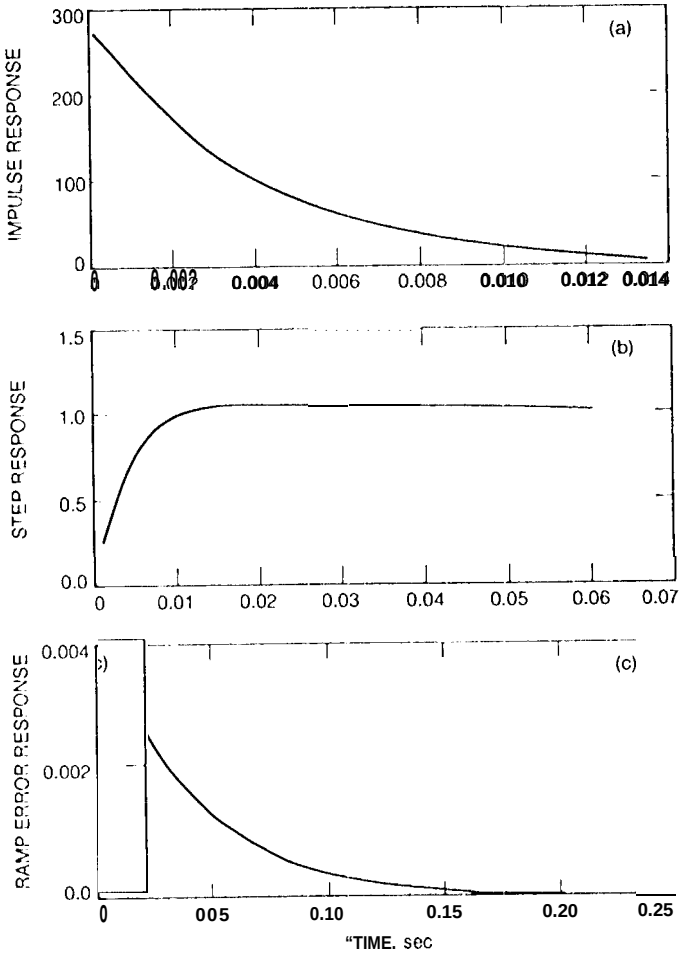


Fig. 5. Time-domain responses of the APLL at strong signal: (a) impulse, (b) step, and (c) ramp error.

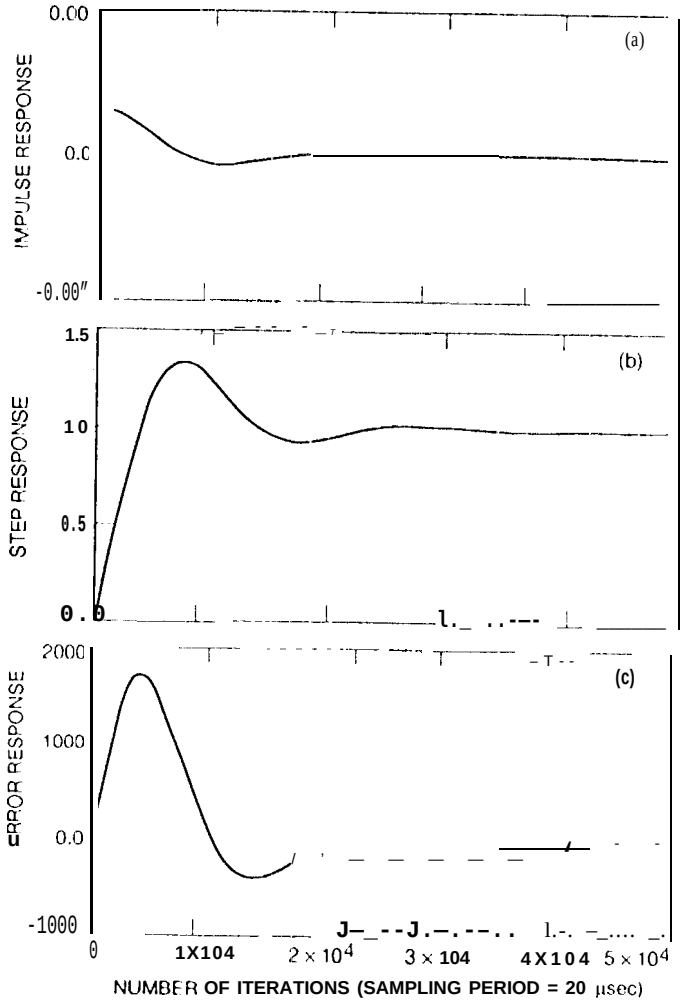


Fig. 6. Responses of the HDPLL at threshold: (a) impulse, . (b) step, and (c) ramp error.

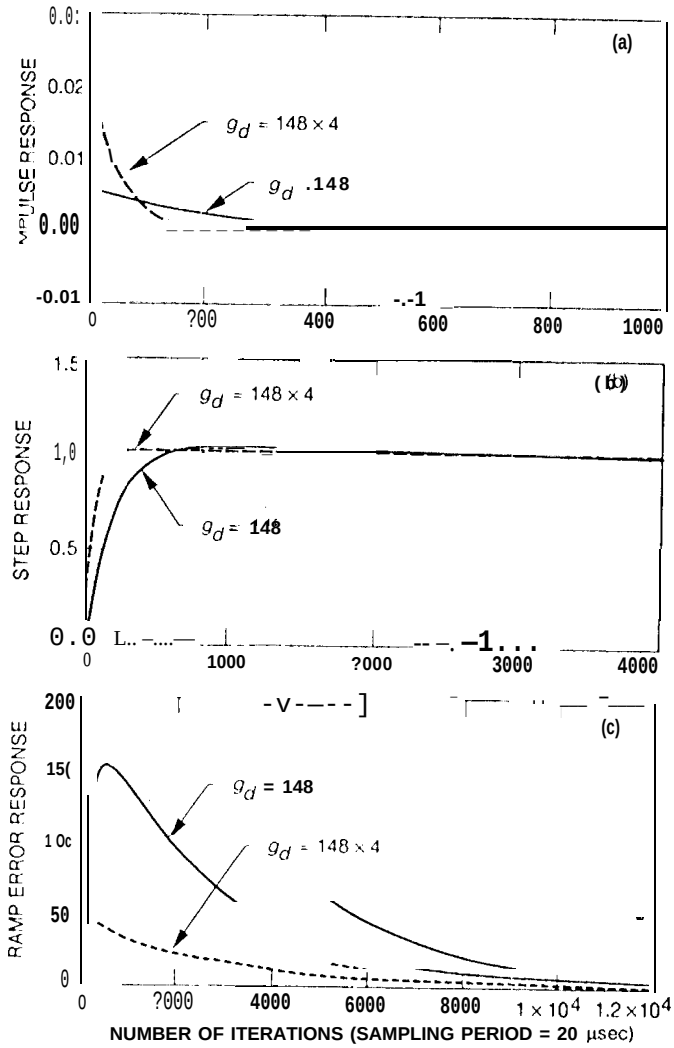


Fig. 7. Responses of the HDPLL at strong signal with two different digital gains: (a) impulse, (b) step, and (c) ramp error.

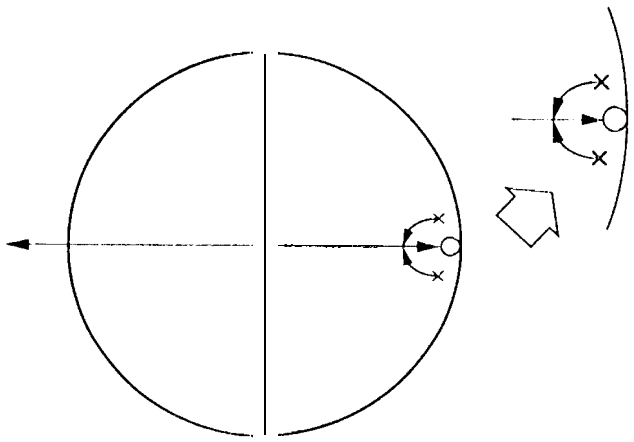


Fig. 8. The root locus plot of the HIDPLL.

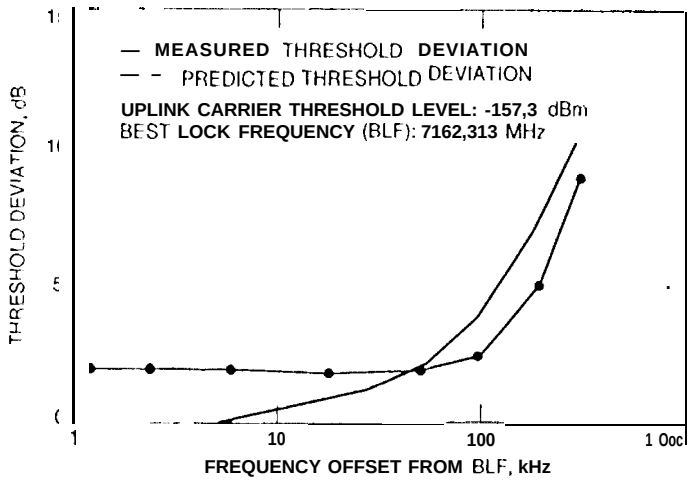


Fig. 10, The measured receiver carrier tracking threshold versus the offset frequency.

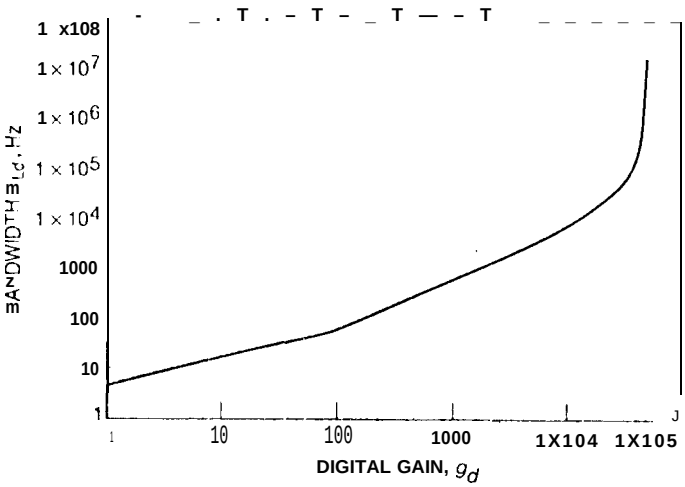


Fig. % Digital gain g_d versus one-sided noise equivalent bandwidth B_{Ld} at strong signal.

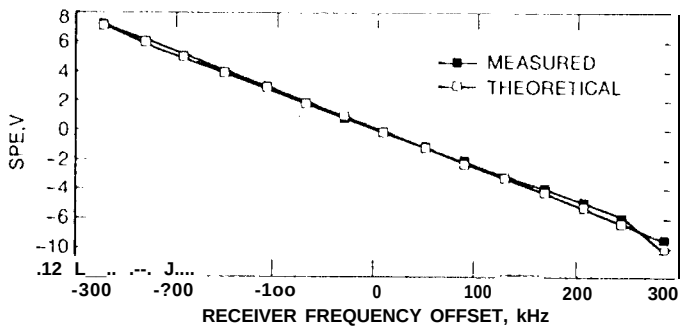


Fig. 11. The measured static phase error voltage of the HDPLL versus uplink frequency offset over the receiver tracking range.

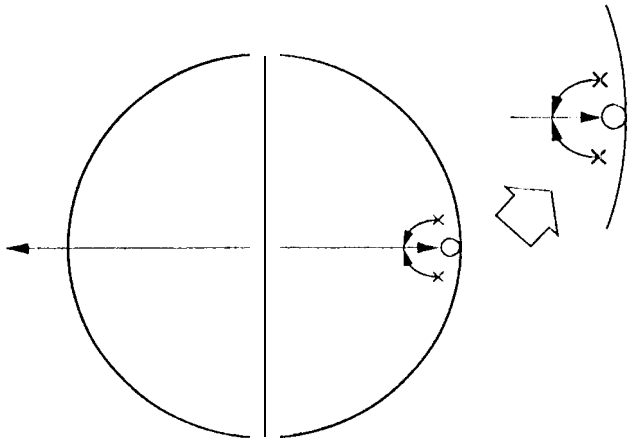
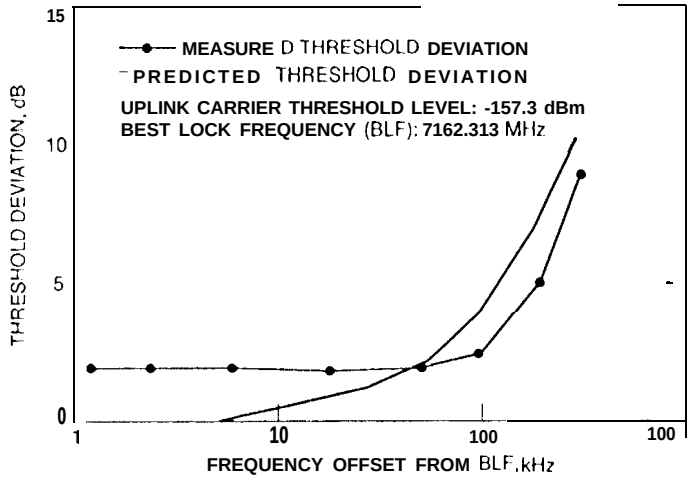


Fig. 8. The root locus plot of the HDPLL.



Fiq. 10. Themeasured receiver carrier tracking threshold versus the offset frequency.

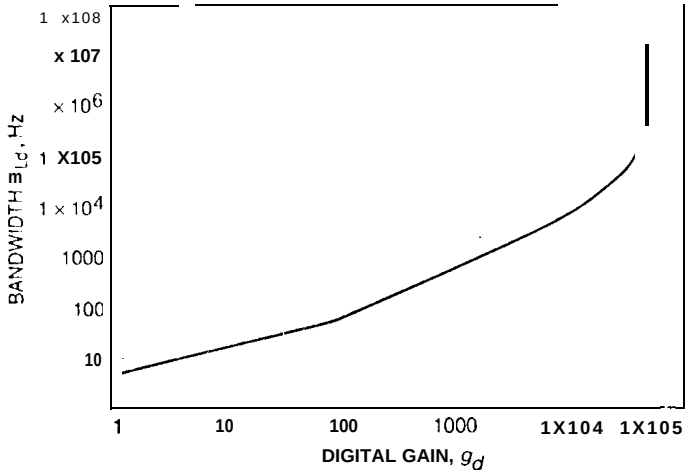


Fig. '9. Digital gain gdversus one-sided noise equivalent bandwidth B_{Ld} at strong signal.

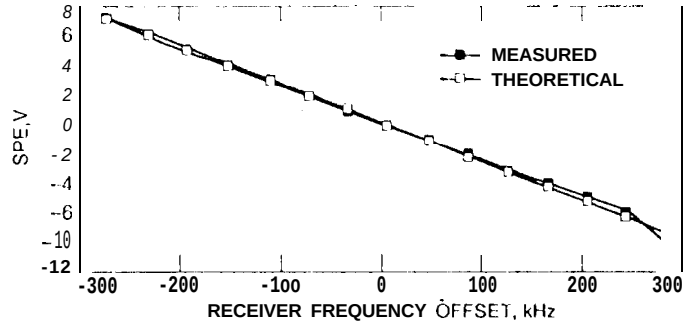


Fig. II. The measured static phase error voltage of the HDPLL versus uplink frequency offset over the receiver tracking range.